ABSTRACT

In some embodiments, a method and apparatus for simulating segmented addressing on a flat memory model architecture are described. In one embodiment, the method includes the translation of instructions from a source instruction set architecture (ISA) having a segmented memory addressing model into a target ISA having a non-segmented memory addressing model. The conversion of instructions into translated instructions for execution within the target ISA is performed by simulating a segmented memory addressing model within the target ISA for the translated instructions. In one embodiment, hardware components and data structures of the target ISA are allocated to simulate the segmented memory addressing model within the target ISA. Accordingly, translated code utilizes allocated flags, such as predicate registers, in order to convert translated program statements having logical address expressions into linear addressing expressions supported by the target ISA. Other embodiments are described and claimed.